What is claimed is:

1. A data processing apparatus comprising:

a CPU configured to operate with one of a plurality of clock frequencies determined in accordance with a selected one of a plurality of clock change signals, a priority order given to the plurality of clock change signals;

a storage unit for storing plural pieces of CPU operating condition setting information corresponding to the plurality of clock change signals, respectively, the plural pieces of CPU operating condition setting information including at least the plurality of clock frequencies, respectively;

a selector for selecting one of the plurality of clock change signals based on the priority order; and

a clock frequency changer for determining the one of the plurality of clock frequencies based on one of the plural pieces of CPU operating condition setting information including the selected one of the plurality of clock change signals.

2. The data processing apparatus according to claim 1 further comprising a detector for determining whether a memory access is currently performed, and wherein the plural pieces of CPU operating condition setting information include a plurality of memory access timings corresponding to the plurality of clock change signals, and the clock frequency changer is inoperative when the detector determines that the memory access is currently performed, and determines the one of the plurality of clock frequencies together with one of the

plurality of memory access timings based on the plural pieces of CPU operating condition setting information when the detector determines that the memory access is currently unperformed.

3. The data processing apparatus according to claim 1, wherein the plurality of clock change signals correspond to a plurality of interrupt signals provided to the CPU, respectively.

4. The data processing apparatus according to claim 2, wherein the plurality of clock change signals correspond to a plurality of interrupt signals provided to the CPU, respectively.

5. The data processing apparatus according to claim 1, wherein the priority order is decided in accordance with a value of a clock frequency determined in connection with each of the plurality of clock change signals.

6. The data processing apparatus according to claim 1 further comprising a clock stop unit for preventing passage of a clock signal to the CPU, and a stop cancellation unit for resuming the passage of the clock signal to the CPU in response to at least one of the plurality of clock change signals.

7. A data processing apparatus comprising:

a CPU configured to operate with one of a plurality of clock frequencies determined in accordance with a selected one of a plurality of clock change signals, a priority order given to the plurality of clock change signals;

storage means for storing plural pieces of CPU operating

condition setting information corresponding to the plurality of clock change signals, respectively, the plural pieces of CPU operating condition setting information including at least the plurality of clock frequencies, respectively;

selecting means for selecting one of the plurality of clock change signals based on the priority order; and

clock frequency changing means for determining the one of the plurality of clock frequencies based on one of the plural pieces of CPU operating condition setting information including the selected one of the plurality of clock change signals.

8. The data processing apparatus according to claim 7 further comprising a detecting means for determining whether a memory access is currently performed, and wherein the plural pieces of CPU operating condition setting information include a plurality of memory access timings corresponding to the plurality of clock change signals, and the clock frequency changing means is inoperative when the detecting means determines that the memory access is currently performed, and determines the one of the plurality of clock frequencies together with one of the plurality of memory access timings based on the plural pieces of CPU operating condition setting information when the detecting means determines that the memory access is currently unperformed.

9. The data processing apparatus according to claim 7, wherein the plurality of clock change signals correspond to a plurality of interrupt signals provided to the CPU, respectively.

10. The data processing apparatus according to claim 8, wherein the plurality of clock change signals correspond to a plurality of interrupt signals provided to the CPU, respectively.

11. The data processing apparatus according to claim 7, wherein the priority order is decided in accordance with a value of a clock frequency determined in connection with each of the plurality of clock change signals.

12. The data processing apparatus according to claim 7 further comprising a clock stop means for preventing passage of a clock signal to the CPU, and a cancellation means for resuming the passage of the clock signal to the CPU in response to at least one of the plurality of clock change signals.